CLAIMS

What is claimed is:

1. A memory cell, comprising:

an insulating layer formed on a first electrode layer, said insulating layer having a first opening;

a stencil layer formed on said insulating layer, and having a second opening formed in an area of said first opening;

a phase-change material layer formed on a surface of said first electrode layer in said first opening; and

an electrically conductive layer comprising a first portion formed on said stencil layer and defining a second electrode layer, and a second portion formed on said phase-change material layer.

2. The memory cell according to claim 1, wherein said second portion of said electrically conductive layer forms a pillar structure which surrounds a sidewall of said phase-change material layer.

3. The memory cell according to claim 2, wherein a bottom of said phase-change material layer is surrounded by said first electrode layer, and a remaining portion of said phase-change material layer is surrounded by said pillar structure.

4. The memory cell according to claim 2, wherein a gap is formed between a sidewall of said pillar structure and said insulating layer to thermally isolate said pillar structure.

5. The memory cell according to claim 1, wherein said stencil layer comprises one of platinum, germanium, and silicon.

6. The memory cell according to claim 1, wherein said first electrode layer comprises a first electrically conductive material and said electrically conductive layer comprises a second electrically conductive material.

7. The memory cell according to claim 6, wherein said first electrically conductive material and said second electrically conductive material comprise different materials, such that a Schottky barrier is formed at an interface of said pillar structure and said first electrode layer.

8. The memory cell according to claim 6, wherein said phase-change material layer comprises a chalcogenide, and said second electrically conductive material is less electrically resistive than an initial as-deposited amorphous phase of said chalcogenide.

9. The memory cell according to claim 6, further comprising:

a third electrically conductive material formed on said first electrode layer in said first opening, said phase-change material layer being formed on said third electrically conductive material, such that said phase-change material layer is surrounded by said second and third electrically conductive materials.

10. The memory cell according to claim 9, wherein said second and third electrically conductive materials comprise a solid solution of Bi_2Te_3 and Sb_2Te_3.

11. The memory cell according to claim 10, wherein said solid solution comprises $Bi_9Sb_{31}Te_{60}$.

12. The memory cell according to claim 7, wherein a temperature change of said phase-change material layer causes a change in a threshold voltage of said Schottky barrier, and

wherein said change in said threshold voltage is used to read out the phase of the phase-change material.

13. A method of fabricating a memory cell, comprising:

forming a first electrode layer using a first electrically conductive material, an insulating layer, and a stencil layer having an opening, in that order, on a substrate;

etching said insulating layer through said opening in said stencil layer, to expose a surface of said first electrode layer;

depositing a phase-change material layer through said opening in said stencil layer onto said surface of said first electrode layer; and

depositing a second electrically conductive material to form a second electrode layer and a pillar structure through said opening on said phase-change material layer, using an spread-angle for deposition which is greater than that for said phase-change material.

14. The method according to claim 13, wherein said etching said insulating layer comprises undercut etching in which a portion of said insulating layer underneath said stencil layer is etched, such that an opening is formed in said insulating layer which has a larger diameter than said opening in said stencil layer.

15. The method according to claim 13, further comprising:

lithographically defining bottom and top electrodes from said first electrically conductive material and said second electrically conductive material, respectively.

16. The method according to claim 13, wherein said second electrically conductive material is deposited using a deposition beam having a spread-angle for deposition which is greater than the spread-angle for deposition for said phase-change material layer by using one of different deposition conditions, and different deposition techniques to form said phase-change material layer and said pillar structure.

17. The method according to claim 13, wherein said phase-change material layer is deposited using a first directional beam, and said second electrically conductive material is deposited using a second directional beam having a broader angle of deposition than said first directional beam.

18. The method according to claim 13, wherein said depositing said phase-change material layer and said depositing said second electrically conductive material comprise providing an angle of deposition by using one of a change in a beam characteristic and a change in substrate orientation.

19. The method according to claim 13, further comprising:

depositing a third electrically conductive material through said opening in said stencil layer onto said first electrode layer, said phase-change material layer being formed on said third electrically conductive material, such that said phase-change material layer is surrounded by said second and third electrically conductive materials.

20. The method according to claim 19, wherein said depositing said phase-change material layer comprises directionally depositing said phase-change material layer, such that said phase-change material layer is deposited off-center from said opening in said stencil layer.

21. The method according to claim 13, wherein said depositing said phase-change material layer comprises directionally depositing said phase-change material layer, such that said phase-change material layer is deposited off-center from said opening in said stencil layer.

22. The memory cell according to claim 1, wherein said phase-change material layer comprises a plurality of phase-change material layers formed in a multi-layer stack.

23. The memory cell according to claim 22, wherein said plurality of phase-change material layers have different phase transition temperatures.

24. The memory cell according to claim 23, wherein said multilayer stack further comprises at least one barrier layer formed between said plurality of phase-change material layers.